DESIGNING OF 4X4 WALLACE TREE MULTIPLIER USING 8T HIGHER ORDER COMPRESSOR


Abstract

This paper is about the designing of Wallace tree high speed 4x4 multiplier that is used in image compression, microprocessor etc. The multiplier is designed by using 8 T adders instead of conventional adder that will leads to lesser power consumption delay and minimized the devices. The simulation has been carried out on Tanner EDA tool on BSIM3V3, 180 nm.

Introduction

With the advancement in mobile communication and image compression techniques in recent trends the emphasis is in modern VLSI design under which main considerations are Power, area and speed. In all the application to VLSI fast speed and small size is required.

There are two basic approaches to improve the speed of multipliers. One is booth algorithm and other is Wallace tree algorithm.

Multipliers require high delay during the partial products addition and conventional multipliers have seven stages so delay is more. But in this paper the work has been done to reduce delay and size hence speed of operation is improved.

The Wallace tree algorithm is employed to design the high speed multiplier and it is a five stage operation which again leads to lesser delay and number of devices. Here compressor are used so number of adders are minimized.

Multiplier

Multiplication is a very common task in modern digital electronics. The two most important methods used is to either perform shift and add operations and use existing components in a CPU, or add a multiplier unit.

Multipliers in digital design are often divided into two subgroups: Array multipliers and tree multipliers. Array multipliers use a rigid pattern to construct their multipliers multiplication process involves multiplication of partial product and higher order addition.

This leads to compact designs and an evenly distributed delay. Tree multipliers on the other hand reduce the number of bits in each level in the tree until the calculation is done.

Since this produces a complex tree structure, the delay is not evenly distributed. This may cause glitches that use power. And the tree structure uses a lot of interconnection; end therefore uses a lot more area. Despite the larger area and not so evenly distributed delay, the tree multipliers use less power than array multipliers. Another advantage tree multiplier have, is that they are a lot faster. The depth of an array multiplier is \(O(n) = n\) while it is \(O(n) = \log_2 n\) for multiplier trees. Even though the wiring cause more delay for multiplier trees, it still perform faster than array multipliers.

3T Xor Gate

The design of 3T full adder is based on the design of the XOR gate. The designing of proposed full adder has been done by using 3T XOR gate as shown in figure 1. The design is based on a modified version of a CMOS inverter and a PMOS pass transistor[2]. When logic high input is provided at B the inverter work as CMOS inverter.

![Fig. 1 Designing of 3T XOR Gate](image)

Therefore the output \(Y\) is the complement of input \(A\). When the input \(B\) is at logic low, the CMOS inverter goes to the high impedance. Whenever, the pass transistor \(M3\) is
enabled and the output Y is equal to input A. Then it works like a 2 input XOR gate. When voltage degradation due to threshold drop occurs across transistor M3, It can be minimized by increasing the W/L ratio of transistor M3.

8T Adder

For the designing of 8T full adder three transistor XOR gate is employed. As the silicon area is very small it is using new version of CMOS invertor and PMOS pass transistor. Boolean expression of 8T full adder is given as:

\[ s = A \oplus B \oplus \text{Cin} \]
\[ \text{Cout} = \text{Cin} (A \oplus B) + AB \]

(1)  
(2)

Schematic of 8 T full adder is shown in Fig. 2. Sum output of full adder is XORing of A, B and Cin.

### 4:3 Compressor

Compressor logic is basically based upon the concept of the counter of full adder. It can be defined as a adder having varying inputs but only three outputs. The three outputs facilitate to count 7. A 4:3 Compressor can be designed using pass transistor logic.

<table>
<thead>
<tr>
<th>Input Condition</th>
<th>Outputs</th>
<th>Decimal</th>
</tr>
</thead>
<tbody>
<tr>
<td>All inputs are zero</td>
<td>X3 X2 X1</td>
<td>0</td>
</tr>
<tr>
<td>Any one input is one</td>
<td>0 0 1</td>
<td>1</td>
</tr>
<tr>
<td>Any two inputs are one</td>
<td>0 1 0</td>
<td>2</td>
</tr>
<tr>
<td>Any three inputs are one</td>
<td>0 1 1</td>
<td>3</td>
</tr>
<tr>
<td>Any four inputs are one</td>
<td>1 0 0</td>
<td>4</td>
</tr>
</tbody>
</table>

Table 1: Counter Property of 4:3 Compressor

![Fig. 3 Modified 4:3 Compressor](image)

### Proposed Algorithms

The algorithm used for multiplier designing in this paper is modified Wallace tree. Wallace suggested the idea of pseudo address[2]. These are the arrays of full adders basically and does not have ripple carry. It takes three inputs and provide two outputs. Pseudo adders are used in summation of several partial products. In first stage, implementation of multiplication is by adding partial products. In first stage,
implementation of multiplication is by adding partial products and these are obtained by conceptually multiplying the Whole multi-digit multiplicand by weighted digit of multiplier. In this way the stages are reduced and the carry look ahead adder (CLA) is used at final stage Wallace trees reduces the number of partial products to two rows of sum and carries.

It is to be mentioned that 4:3 compressors has three outputs of bit position jth, (j+1)th and (j+2)th. If a compressor is used in column no four then it’s jth output goes to the circuit of column no fifth and (j+1)th bit goes to the circuit of column no six and the rest output goes to the circuit of column no seven of the next stage. Thus our compressors reduce vertical critical path more rapidly than conventional compressors [1].

In this multiplier we have used 8 T full adders, 4:3 Compressor and half adder. A little modification has been done in Wallace tree algorithm it is observed that stages and number of transistors are also reduced.

Designing, Synthesis and Results

The schematic of proposed 4x4 multiplier is shown in Fig. and its simulation has been carried out in 180ns EDA Tanner tool. The output waveforms are also shown in Fig. As we have designed the multiplier using 8 T full Adder hence small voltage degradation for some input combinations and these degradation has been minimized by employing CMOS inverters as level resistors at appropriate places in the circuit.
Conclusion

In this paper we have designed 4x4 multiplier using 8T full adder. For the designing of multiplier 8T full adder, 3T XOR, 4:3 compressor has been used. Wallace tree algorithm is used for the step reduction purpose. The proposed multiplier has a much less delay and hence much less power delay product and number of devices used are reduced to the great extent. As the multiplication steps are reduced a lot hence speed of multiplier is enhanced.

References


Biographies

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