CROSSTALK NOISE AND DELAY REDUCTION IN VLSI INTERCONNECTS

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Abstract

Crosstalk in interconnects had a great impact on overall reliability and performance of IC and thus it plays a key role in deep submicron (DSM) VLSI circuits.In this paper schmitt trigger is designed as a buffer which operates at a 20 GHz frequency so as to minimize crosstalk noise and delay in interconnects. In order to propagate the signal with the reduced noise and delay simultaneous buffer and wire sizing is done along with buffer insertion through interconnects .Accurate SPICE results shows that at 90nm technology node crosstalk noise is reduced by 60% and delay by 56% for 1V power supply.

Keywords-crosstalk noise, delay, buffer insertion.

Introduction

The increase of integration density in submicron designs contributes to the greater proximity of adjacent wires on the same layer with higher aspect ratio, thus it results in an increase of crosstalk noise and delay. Due to mutual coupling capacitance between two neighboring wires, unwanted crosstalk noise is produced. For example, when two wires are placed adjacently they form a coupling capacitor and a mutual inductor and thus a current or a voltage change on one wire can interfere the signal on the other wire resulting in crosstalk. The inductive effects must be considered at higher frequencies increasing above 500MHz [1].

The interaction between signals on two different electrical wires leads to crosstalk. One of the wire creating crosstalk is called an “aggressor”, and the one receiving effect is called a “victim”. A wire can be an aggressor as well as a victim. The RC delay of the interconnect should be reduced so as to increase the operating speed of an integrated circuit. The interconnect resistance (R) and interconnect capacitance (C) increases linearly with increase in interconnect length, making the RC delay to increase quadratically[2].Along with increased signal propagation delay, increased power dissipation is another effect of large interconnect impedance. The total signal propagation (RC) delay of an interconnect can be reduced with the repeater insertion operating at a higher frequency. In CMOS technology, the simplest form of a repeater consists of two transistor (PMOS and NMOS) inverter. The objective of the paper is to design a buffer operating at 20GHz frequency and to insert the buffer for the purpose to reduce delay, power and noise in VLSI interconnects.

In this paper, Schmitt trigger as a buffer is designed to operate at a higher frequency so as to reduce delay and power in interconnects along with transmission of signals at a higher rate[3]. In Comparison with the ordinary CMOS buffer, a Schmitt trigger switches fastly .Thus it leads to the reduction in delay .Coupling noise is reduced by simultaneous buffer and wire sizing. The organization of the paper is as follows.Section 2 will provide an overview of the buffer designing, buffer insertion, and driver and interconnect sizing.Section 3 describes the results and discussions by applying a wire and buffer sizing methodology to a 90nm technology node. Finally conclusions will be given in section 4.

Our Approach

In this section we discuss designing of a buffer at 20GHz frequency, buffer insertion and wire sizing so as to reduce crosstalk noise and delay. Here Schmitt Trigger is used as a buffer as shown in Figure.1.

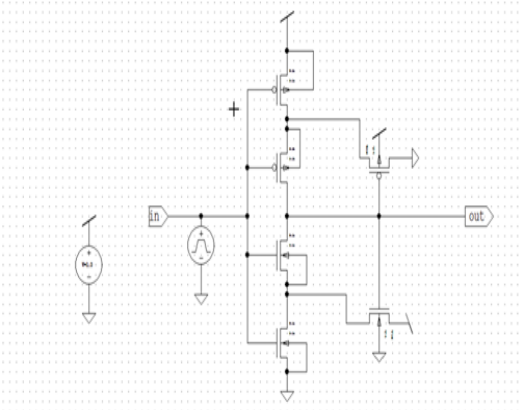

Figure 1: Schmitt trigger as a buffer.

Figure.1 describes Schmiit Trigger as a buffer which

consists of PMOS and NMOS transistor.Width of PMOS is 3 times the width of NMOS.

$$W_p = 3W_n \quad (1)$$

The reason behind designing this Schmitt trigger is that it responds faster to an input signal transition than a simple CMOS buffer.

The designed Schmitt trigger buffer is inserted through an interconnect length so as to exactly propagate the signal from transmitting to receiving end at a higher frequency.

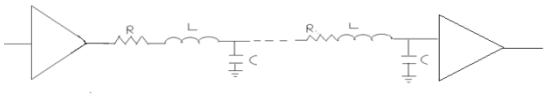

Figure 2: Buffers inserted in an RC interconnect model

Crosstalk noise and delay can be reduced through buffer insertion and wire sizing. In addition to this, power consumption is also reduced. However, using Schmitt Trigger as a buffer results in an increase in area.

Consider two interconnect i and j with width w and height h, separation between two interconnects is s, t is the thickness of the dielectric and l is length of the interconnect, the interconnect resistance R is expressed as

$$R=\rho l/wh \quad (2)$$

Where ρ stands for resistivity of the material. interconnect capacitance C can be expressed as

$$C=K\epsilon_{ox}l \quad (3)$$

Where K is a constant and ϵ_{ox} is the oxide permittivity[4]. The RC interconnect delay is 0:377RCl^2 .Thus the delay is proportional to the square of the wire length l. Hence by dividing the interconnect into k segments with repeaters, the interconnect delay term is reduced to 0:377RCl^2/K. However, these repeaters can introduce additional gate delay. Optimal sizing and number of the repeaters can be determined to achieve the minimum delay [5].The optimum number of repeaters k_{opt-RC} and the optimum repeater size h_{opt-RC} can be calculated from the following expressions.

$$k_{opt-RC}(W_{int}) = \sqrt{\frac{R_{int}(W_{int})\ C_{int}(W_{int})}{2.3\ R_oC_o}} * \frac{1}{[1+0.16(T_{Lint/R_{int}}(W_{int})^3)]^{0.24}} \quad (4)$$

$$h_{opt-RC}(W_{int}) = \sqrt{\frac{R_o\ C_{int}(W_{int})}{R_{int}(W_{int})C_o}} * \frac{1}{[1+0.16(T_{Lint/R_{int}}(W_{int})^3)]^{0.3}} \quad (5)$$

$$T_{L_{int}/R_{int}}(W_{int}) = \sqrt{\frac{L_{int}(W_{int})/R_{int}(W_{int})}{R_oC_O}} \quad (6)$$

C_o and R_o are the input capacitance and output resistance of a minimum size repeater respectively.R_{int} (W_{int}) and C_{int} (W_{int}) are the interconnect line resistance and capacitance as functions of interconnect width[5].

Results

At 90nm technology node and 1V power supply the buffer is designed with an operating frequency of 20 GHz. The input and output simulation waveform for the buffer is shown in Figure.3.

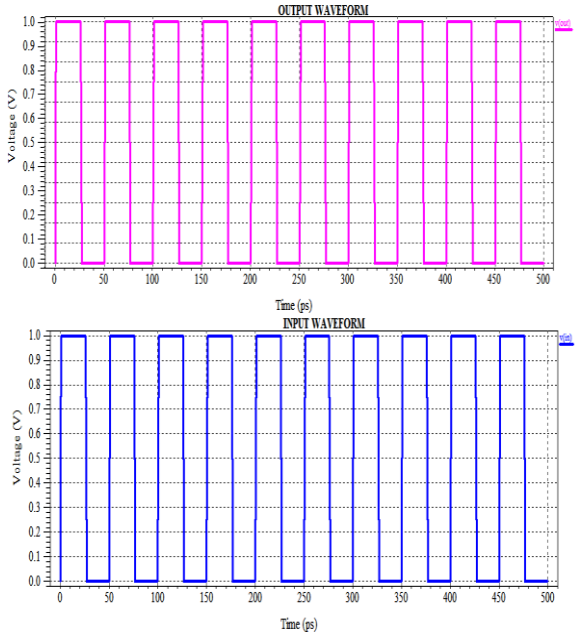

Fig. 3. Input and Output Waveforms of a Buffer.

When input pulse ranging from 0 to 1V is applied to buffer , square wave output is obtained with the same voltage range. The simulation results are calculated for a time period of 500ps.

The parameters used for the designing of buffer are specified in the Table.1.

Table.1 Specifications of the Buffer

Technology used	90nm
Supply Voltage	1.0V,0.8V
Rise time	0.001n
frequency	20GHz
Average power consumed	3.492109e-009 watts

The high frequency buffer is inserted through an interconnect and is operated at 1V supply, signal propagated from input to output with a certain delay as shown in Figure.4 and 5.

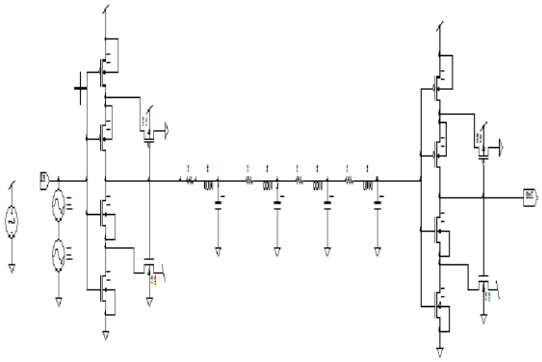

Fig.4. Interconnect with Buffer Insertion.

Figure.4 describes buffer insertion through interconnect. The output simulation waveform shown in Figure.5 is obtained with a certain delay of 50 ps.

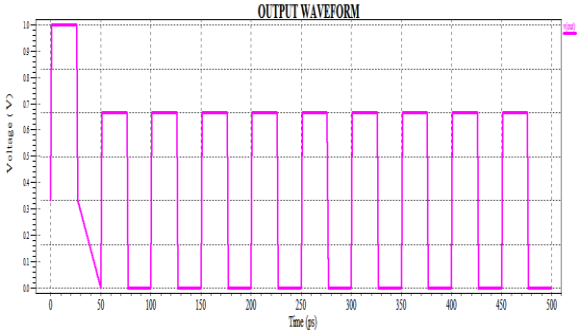

Fig. 5. Output Waveforms With Buffer Insertion.

The average power consumed is 6.565955e-005 watts with delay of 50ps.

As the signal through an interconnect is propagating with a delay from input to the output ,buffer sizing / insertion as well as interconnect sizing is done using closed form solution. The wire sizing can be calculated from the following expression[7].

For any segment i of a wire , $1 \leq i \leq n$,where n is the total number of segments of a wire .

$$h_i = \sqrt{\frac{r_o C_D}{c_o R_u}} \qquad (6)$$

where R_u and C_D are the upstream resistance and downstream capacitance of segment i respectively.

Thus the output obtained after buffer and wire sizing is obtained with less delay as shown in Figure. 6 and 7.

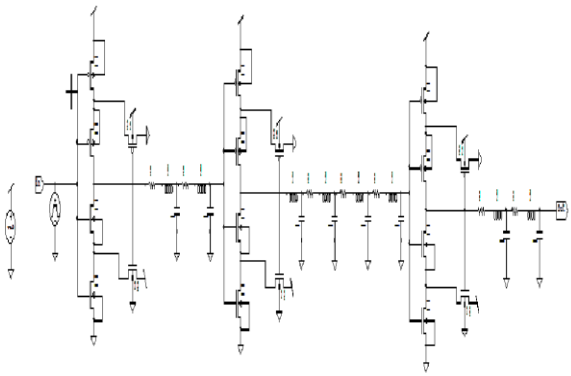

Fig.6 Buffer and Interconnect Sizing.

Figure.6 describes buffer and wire sizing. Interconnect length is divided into segments. Alongwith this, buffer insertion and sizing is done through interconnects so as to reduce the delay.

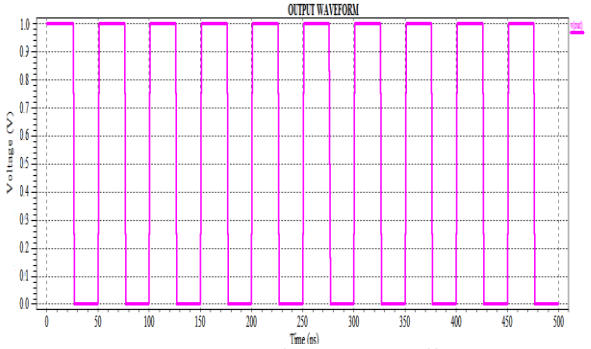

Fig.7. Input and Output Waveforms with buffer and interconnect sizing.

The delay calculated after buffer and wire sizing is reduced to 22ps.The noise for the interconnect after buffer and wire sizing is calculated to be approximately 2.96mV.

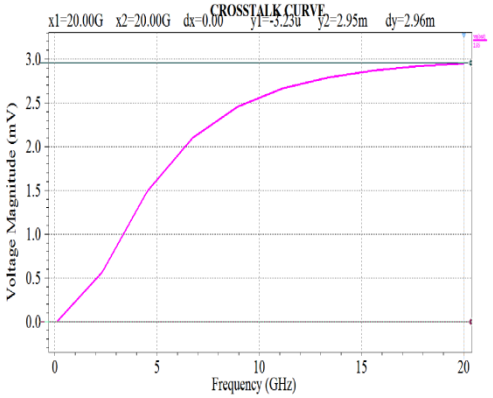

Fig. 8. Noise curve calculated with Buffer and Interconnect Sizing.

Table2. Specifications of the Interconnect with Buffer Insertion/Sizing and Wire Sizing.

Technology used	0.1um
Supply voltage	1.0V
Rise time	0.001n
frequency	20 GHz
delay	22ps
noise	2.96mV
Average power consumed	1.820624e-007 watts

The crosstalk noise calculated between two interconnects after buffer and wire sizing is calculated to be 3.61mV.

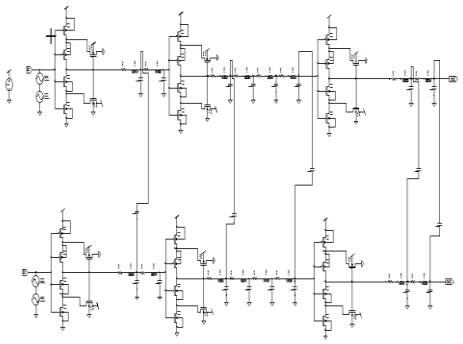

Fig. 9. Crosstalk Noise between two interconnects with buffer and wire sizing.

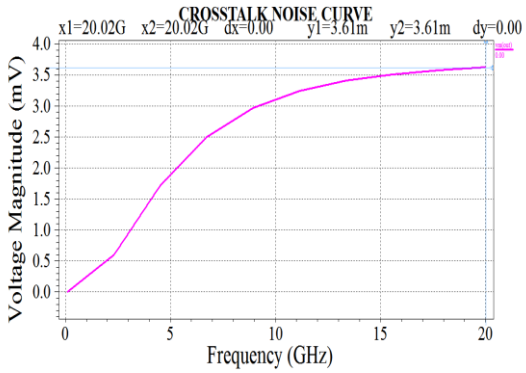

Fig.10. Noise curve calculated with Buffer and wire Sizing between two interconnects.

Thus, Crosstalk Noise and delay is reduced so as to improve the signal propagation from input to the output.

Conclusion

In order to reduce crosstalk noise ,buffer operating at 20GHz frequency is proposed alongwith buffer insertion /sizing and wire sizing so as to reduce the crosstalk noise .In addition to this,the proposed buffer also helps to reduce delay and power. We have observed that crosstalk noise is effectively reduced by 60% and delay is reduced by 56%. Through the various results obtained using SPICE at 90nm technology node we were able to analyze and reduce crosstalk through different techniques such as driver sizing, by varying interconnect length and by designing buffer operating at a higher frequency.

Acknowledgment

I am greatly indebted to my advisor Mrs V.Sulochna Verma for their valuable guidance, consistent encouragement and emphasis on the quality of the research contribution. Finally, and most importantly I would like to thank my family and friends for their support and unconditional love I have enjoyed throughout my life.

References

[1] Fargol Hasani, "Crosstalk and Delay Optimization Techniques for Nano Scale Interconnects" International Conference on Design & Technology of Integrated Systems in Nanoscale Era, 2007.

[2] Saini.S, "Schmitt Trigger as an alternative to Buffer Insertion for Delay and Power Reduction in VLSI Interconnects", IEEE Region10Conference-TENCON, 2009.

[3] Saini .S, "An Alternative approach to buffer Insertion for Delay and Power Reduction in VLSI Interconnects"

[4] Saini Sandeep " A Novel Approach to reduce Delay and Power in VLSI Interconnect", M.S. Thesis Electronics and Communication Engineering, 2009.

[5] A. Mezhiba and E. G Friedman, "Frequency Characteristics of High Speed Power Distribution Networks," Analog Integrated Circuits and Signal Processing,Vol. 35, No. 2/3, pp. 207-214, May/June 2003.

[6] Vani Prasad, "Interconnect Minimization using a Novel Pre-Mid-Post Buffer Strategy", International Conference on VLSI Design IEEE, 2003

[7] Chris C. N. Chu, "Closed Form Solution to Simultaneous Buffer Insertion/Sizing and Wire Sizing" Proceedings of the international symposium on Physical design, 1997.

[8] Jason Kong, "Simultaneous Driver and Wire Sizing" IEEE Transaction on Very Large Scale Integration (VLSI) Systems, 2004.

[9] Iris HuiRuJiang, "Crosstalk Driven Interconnect Optimization By Simultaneous Gate And Wire Sizing",IEEE

Transactions on computer-aided design of integrated circuits and systems, Vol. 19, Issue No. 9, September 2002.

[10] National Technology Roadmap for Semiconductors. Semiconductor Industry Association, San Jose, CA 1997

Bibliographies

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