STUDY ON FUNCTIONAL ANALYSIS AND COMPARISON OF DDRX SDRAM SERIES

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Abstract

Double Data Rate (DDR) SDRAMs have been prevalent in the PC memory market in recent years and are widely used for networking systems. The demand for faster and cheaper memories has been increasing by the day. Hence, these memory devices are rapidly developing to give high density and high memory bandwidths. However, with the increase in technology, complexity of instructions to control the memory devices also increases. In this paper, a comprehensive analysis and comparison of DDR DSRAM, DDR2 and DDR3 are described. Also the advantages of DDR3 over DDR2 and DDR are discussed.

Introduction

The first evolutional advance in DDR SDRAM technologies was the upgrade from DDR to DDR2. The first samples of DDR operated just at 100 MHz (DDR-200), and then the frequency gradually grew to 200 MHz (DDR-400). At the same time latencies were reduced - initial 3-3-3-8 timings changed to 2-2-2-5. Then there appeared higher-frequency DDR memory modules (up to 300 MHz, that is DDR-600), but they were not officially accepted by the JEDEC standard[1]. Increasing memory frequency or reducing latencies required increasing memory voltage from 2.5V to about 2.85V. The problem of excessive heat release was usually solved by using usual heat spreaders.

When further increase in DDR memory frequency was practically impossible, there appeared the second generation of DDR SDRAM desktop memory - DDR2. It gradually proved it competitiveness and replaced the old generation of DDR memory. Initial modifications of DDR2 memory were represented by 200 MHz

(DDR2-400) and 266 MHz (DDR2-533) models - DDR2 started to evolve from the point where DDR (officially) ended its existence. Moreover, the initial DDR2 standard provided for memory modules of much higher frequencies than usual DDR - 333 MHz DDR2-667 modules and 400 MHz DDR2-800 modules. DDR2 chips were based on the new process technology, which allowed to power memory from just 1.8V (one of the power saving factors) and to reach higher memory capacities.

DDR SDRAM

Memory chips transfer data to a memory controller via the external data bus on the rising and falling edge of the clock. That's the essence of the Double Data Rate technology. That's why the rating or the effective frequency of DDR memory is always doubled (for example, DDR-400 at 200 MHz data bus). So, the efficient frequency of the DDR-400 data bus is 400 MHz, while its true clock rate (IO buffer frequency) is 200 MHz Internal clock rate of DDR memory chips (the first generation) equals the true clock rate of the external bus (IO buffer frequency) - 200 MHz for the DDR-400 memory chip[2]. In order to transfer 1 bit per clock (via each data line) along the external bus operating at the effective clock rate of 400 MHz, 2 bits must be transferred per clock of the internal 200 MHz data bus. In other words, we can say that all other things being equal, the internal data bus must be twice as wide as the external data bus. This data access scheme is called *2n*-prefetch.

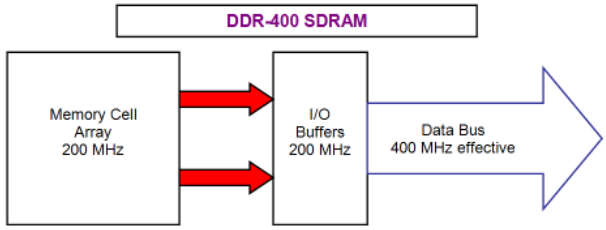

Figure 1 - DDR SDRAM

DDR2 SDRAM

The most natural solution to this problem of obtaining higher clock rates in DDR2 was to reduce the clock rate of the internal data bus to a half relative to the real clock rate of the external data bus (IO buffer frequency). For example, in case of DDR2-800 memory chips (figure 2), IO buffer frequency is 400 MHz, and the efficient clock rate of the external data bus is 800 MHz (because Double Data Rate is still in force - data are still transferred both on the rising and falling edge of the clock). Clock rate of the internal data bus is just 200 MHz, so in order to transfer 1 bit (via each data line) per clock of the external data bus operating at the efficient clock rate of 800 MHz, 4 bits must be transferred per clock of the internal 200 MHz data bus. In other words, an internal data bus of DDR2 must be four times as wide as its external bus[3]. This data access scheme, implemented in

DDR2, is called *4n*-prefetch. It has evident advantages over *2n*-prefetch in DDR.

On one hand, one can use twice as low internal clock rate of memory chips (200 MHz for DDR-400 and just 100 MHz for DDR2-400, which significantly reduces power consumption) to obtain equal peak memory bandwidth. On the other hand, the internal clock rate of DDR and DDR2 memory chips being equal (200 MHz for DDR-400 and DDR2-800), the latter will have twice as high theoretical bandwidth. But its drawbacks are evident as well - DDR2 chips operate at a twice as low clock rate (with the theoretical bandwidth of DDR and DDR2 being equal) and use a more complex 4-1 conversion, which results in noticeably higher latencies. We saw it in practice, when we tested the first samples of DDR2 memory.

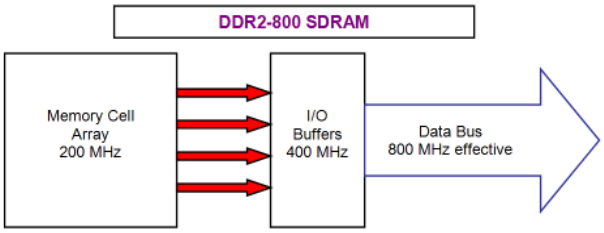

Figure 2 – DDR2 SDRAM

DDR3 SDRAM

It's easy to guess that the DDR2-DDR3 upgrade is based on the same principle as the DDR-DDR2 upgrade. Namely, DDR3 is still DDR SDRAM. That is data are still transferred both on the rising and falling edge of the clock at the doubled effective frequency relative to the memory bus clock rate. Only performance ratings have grown twice as high versus DDR2 - typical performance categories of new DDR3 memory will vary from DDR3-800 to DDR3-1600 (and probably higher). The next doubling of theoretical memory bandwidth has again to do with halving of their internal clock rate. That's why in order to reach the data transfer rate of 1 bit per clock along each line of the external data bus operating at the effective frequency of 1600 MHz (as in Picture 3); 200 MHz chips must transfer 8 bits per clock. That is the internal data bus of memory chips will be eight times as wide as their external data bus. This data transfer scheme with "8-1" conversion will evidently be called *8n*-prefetch[4][5]. Advantages of the DDR2-DDR3 upgrade will be the same as in case of the previous DDR-DDR2 upgrade: on one hand, it's a reduction of memory power consumption while preserving peak memory bandwidth (DDR3-800 versus DDR2-800); on the other hand, it's an opportunity to increase memory clock rates and theoretical bandwidth and retain the old level of the internal clock rate (DDR3-1600 versus DDR2-800). Drawbacks will also be the same - a wider gap between the internal and external clock rates of memory buses will result in higher latencies. It's logical to assume that the relative increase in latencies during the DDR2-DDR3 upgrade will be similar to that of the DDR-DDR2 upgrade.

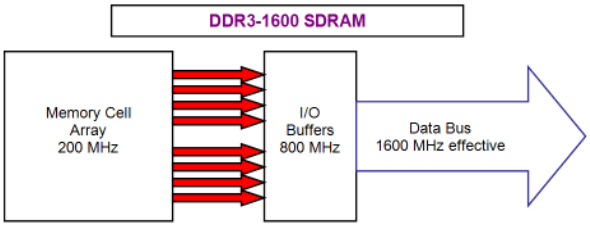

Figure 3 – DDR3 SDRAM

Register definition

There are basically four mode registers in DDR3 SDRAM namely MR0, MR1, MR2 and MR3. Figure 4. Shows MR0 definition where it defines the burst length by MR0[1:0]. The eighth bit is used to change the value of DLL RESET. The PD(Pre-charge) bit is applied only when pre-charge power- down mode is used. CAS Latency is the delay in clock, cycles, between internal READ command and the availability of the first bit of output data

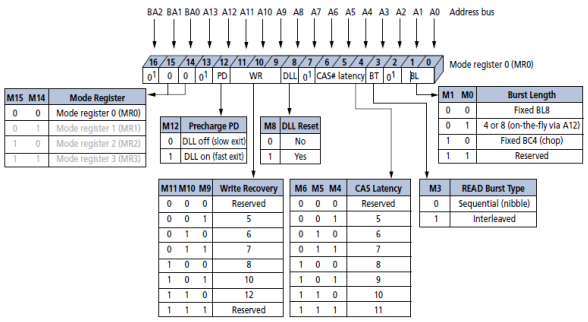

Figure 4 – MR0 register

Memory Register (MR)

The definition for MR1 is described in Figure 5. This mode register controls additional functions and features such as Q OFF (OUTPUT DISALBE), TQDS (Termination data strobe), WRITE LEVELING (which is used during initialization to deskew the DQS for better integrity)[6].

MR2 further controls functions like CAS WRITE Latency(It is the delay in clock cycles from the releasing of the internal write to the latching of the first data in), AUTO SELF REFRESH (ASR), SELF- REFRESH TEMPERATURE (SRT). This is shown in Figure 6.

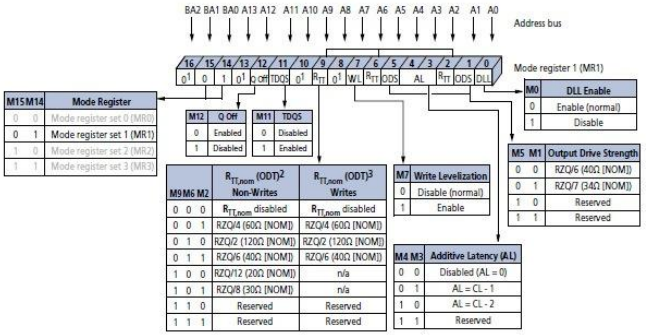

Figure 5 – MR1 register

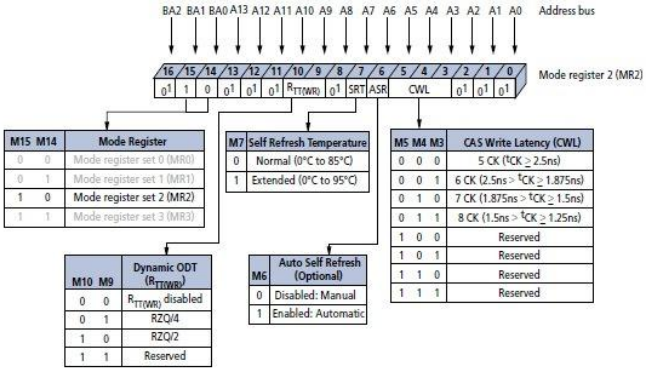

Figure 6 – MR2 register

The MR3 is current defined as the MULTIPURPOSE REGISTER. Its function is to output a predefined system timing calibration bit sequence[6]. This definition is illustrated in Figure 7.

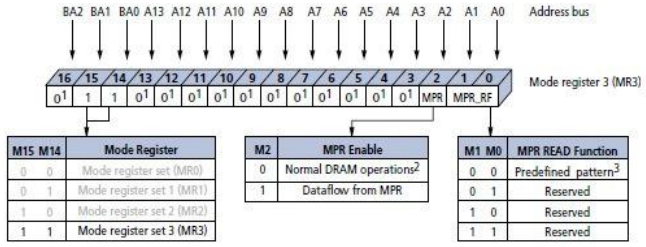

Figure 7 – MR3 register

DDR3 Features Comparison

DDR3 is the next-generation, high-performance solution for CPU systems it pushes the envelope in key areas like power consumption, signaling speeds, and bandwidth, bringing new levels of performance to desktop, notebook, and server computing. DDR3 offers a substantial performance improvement over the previous DDR2 and DDR memory systems. One of the main DDR3 features include improved signal integrity so as to have higher performance without an undue burden on the system designer[7]. Table 1 compares some differences between DDR3 and the previous two.

Table 1- DDR3 Feature Comparison

Feature	DDR SDRAM	DDR2 SDRAM	DDR3 SDRAM	DDR3 SDRAM advantage
Voltage	2.5 V	1.8 V	1.5 V	Reduces memory system power demand from DDR or DDR2 by 17%
Density	64 MB to 1 GB	256 MB to 4 GB	512 MB to 8 GB	High density components simplify memory sub-system
Internal banks	4 (fixed no of rows and columns)	4 and 8	8	Has higher page-to-hit ratio and better maximum thoroughput.
Bank interleaving	--	Allows Bank interleaving	Allows Bank interleaving	It is extremely effective for concurrent operations and can hide the timing overhead.
Prefetch	2	4	8	Lower memory core speed results in higher frequency and lower power operation.
Speed	100 to 200 MHz	200 to 533 MHz	300 to 1066 MHz	Higher data rate.
Maximum frequency	200 MHz or 400 Mbps per DQ pin	533 MHz or 1066 Mbps per DQ pin	1066 MHz or 2133 Mbps per DQ pin	Higher data rate.
Read latency	2, 2.5 ,3, clocks	3, 4, 5 clocks	5, 6, 7, 8, 9, 10 and 11	Eliminating half clock setting allows 8n prefetch architecture.
Additive latency	--	0, 1, 2, 3, 4	0, CL1 or CL2	Improves command efficiency.

Conclusion

DDR2 gradually proved it competitiveness and replaced the old generation of DDR memory. Initial modifications of DDR2 memory were represented by 200 MHz . Double Data Rate (DDR) SDRAMs have been prevalent in the PC memory market in recent years and are widely used for networking systems. These memory devices are rapidly developing, with high density, high memory bandwidth and low device cost. However, because of the high-speed interface technology and complex instruction-based memory access control, a specific purpose memory controller is necessary for optimizing the memory access trade off.

Acknowledgment

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