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# Optimization Design Techniques for Reduce Power Consumption in CMOS Circuit for VLSI Design

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## Abstract

Power dissipation becoming a limiting factor in VLSI circuits and systems. Due to relatively high complexity of VLSI systems used in various applications, the power dissipation in CMOS inverter, arises from it's switching activity, which is mainly influenced by the supply voltage and effective capacitance. One of challenge with technology scaling is the rapid increase in subthreshold leakage power due to Vt reduction. Leakage power dissipation is a component of static power dissipation in CMOS circuits. It is caused by the presence of leakage currents in the MOS transistors. Leakage power can be reduce by Stack, Sleep and Sleepy keeper transistor techniques. Sleepy Keeper technique provided lesser static power dissipation and lesser static power delay product in comparison with the other techniques. The main advantage of using Sleepy Keeper technique is that it retains the logic state and also lowers the subthreshold leakage power dissipation. It has been shown previously that the stacking of two off transistors has significantly reduced sub-threshold leakage compared to a single off transistor. In stack transistor technique two half channel width transistors are connected in series to for one of the transistor in pull up and pull down networks with gates to increase the stack effect, it will increase the resistance between the supply and ground. Therefore, the leakage of the logic gate is reduced. A MOS transistor in the circuit is divided and stacked into two half width size transistors. When two half size stacked MOS transistors are turned off together, induce reverse bias between them results in the reduction of the sub threshold leakage power. However, increase in the number of transistors increases the overall propagation delay of the circuit. In this work we analyze the parametric estimation for MOSFET switching delay, leakage current reduction, power dissipation and variation of temperature effects due to the parasitic devices. One solution to the problem of ever-increasing leakage is to force a non-stack device to a stack of two devices without affecting the input load. The stacking of two off devices has significantly reduced sub-threshold leakage compared to a single off device. Logic gates after stack forcing will reduce leakage power, but incur a delay penalty which is improve in our work, similar to replacing a low- Vt device with a high- Vt device in a dual- Vt design. Due to stacking of devices, the drive current of a forced-stack gate will be lower resulting in increased delay. Here we can design a full adder logic circuit using stack transistors.

**Keywords:** Low power, power dispassion, energy efficient, source leakage current, gate current, switching power, gate capacitance, power reduction.

## INTRODUCTION

Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching and static power is consumed regardless of transistor switching. Dynamic power consumption was previously (at 0.18- m technology and above) the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. Therefore, many previously proposed techniques, such as voltage and frequency scaling, focused on dynamic power reduction. However, as the feature size shrinks, e.g., to 0.09 and 0.065 m, static power has become a great challenge for current and future technologies.In the last few years, many researchers have focused their efforts on the design of ultralow-power systems, such as battery-powered portable devices , energy scavenging sensors networks, and devices for biomedical or environmental monitoring. One of the widely used techniques to minimize power consumption consists in supplying circuits with a voltage lower than the threshold voltage of the transistors. Determining the value Vmin of the supply voltage Vdd at which the minimum energy consumption is achieved without compromising the correct running of a circuit is not trivial. Moreover, in order to obtain an estimation of Vmin as precise as possible, process variations must be also taken into account, since process variations in the subthreshold regime are very severe and can cause up to a 300% gate delay variation.Due to the robust nature of static CMOS logic, circuits in this technology family can operate with supply voltages below the transistor threshold voltage (Vth), while consuming orders of magnitude less power than in the normal strong-inversion region. The operating frequency of subthreshold logic is much lower than that of regular strong inversion circuits (Vdd > Vth) due to

the small transistor current, which consists entirely of leakage current. The lowoperating frequency and low supply voltage combine to reduce both dynamic and leakage power, leading to the significant power savings seen in subthreshold designs. The characteristics of MOS transistors in the subthreshold region are significantly different from those in the strong inversion region. The saturation current, which was a near-linear function of the gate and threshold voltages in the strong inversion

# THE HISTORY AND TREND OF POWER DESIPATION OF DIFFERENT COMPONENET OF CMOS

For several decades Moore's law has served as a beacon to predict device density and its sub sequent power dissipation. According to Moore's law semiconductor transistor density and performance doubles for every 18 months. This prediction was done in 1970's the chip complexity chart below shows the trend in transistor integration on a single chip over more than the past two decades fig(1)

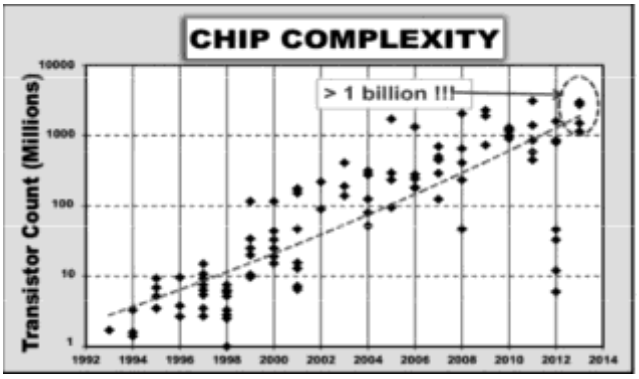



**Fig1: Chip complexity and trend in transistor integration over more than 2 decades.**

Power dissipation has propelled due to transistor scaling, chip transistor count and due to clock frequencies. Sophisticated strategies to lower leakage and manage voltage and variability have strengthened in total power consumption. Since power reduction is mandatory in each application the trend for adjusting near constant clock frequencies also continues as shown below in frequency trend plot. Fig(2).

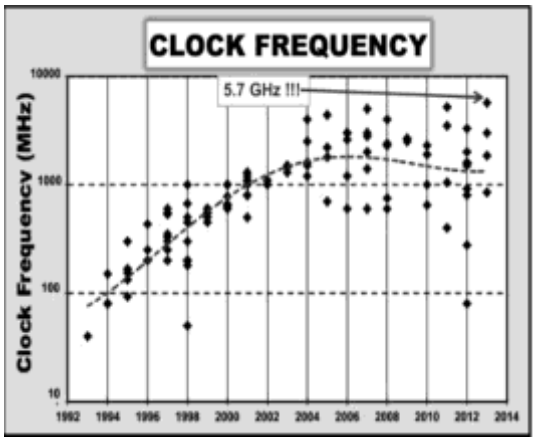
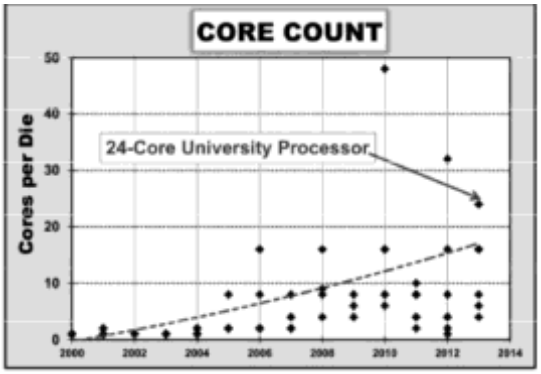



**Fig2: Clock frequency Trend**

Processors are choosing to trade off performance by reducing supply voltage. The performance loss due to voltage and clock frequency reduction is compensated by further increasing parallelism in the processor. As of today devices are having more than 8 core processors. The respective chart is given below. Fig (3)




**Fig(3): core count**

In addition to the trend to integrate more cores on a single chip and multiple die within a single package large cache integration was done as shown in fig(4)

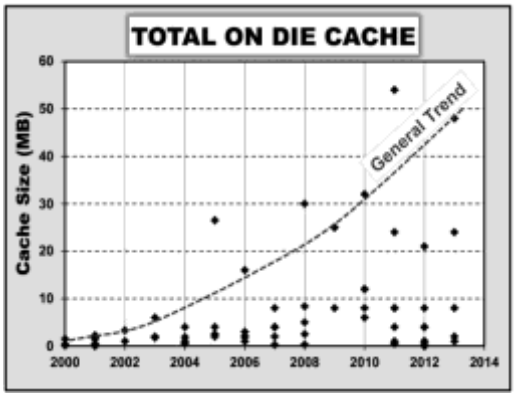



**Fig (4): Cache capacity**

In early electronics era power dissipation was very high since most of the devices contained only bipolar junction transistors this lead to the introduction of CMOS. The power dispassion comparison graph given below Fig(5)

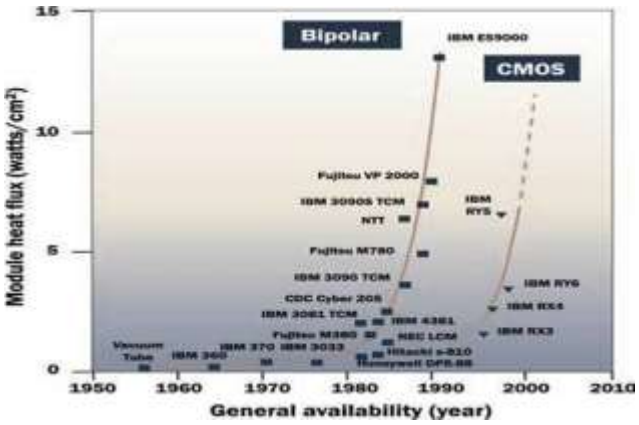



**Fig (5): Comparison of CMOS and BJT's power dissipation.**

# MECHANISMS OF POWER DESSIPATIONS

Mechanisms of power dissipation are divided into two classes: dynamic and static power dissipation. Dynamic dissipation of power mainly occurs operational mode of the circuit eg. When the circuit is performing some other operation on the data. Static power dissipation becomes an issue when circuit is in inactive mode.

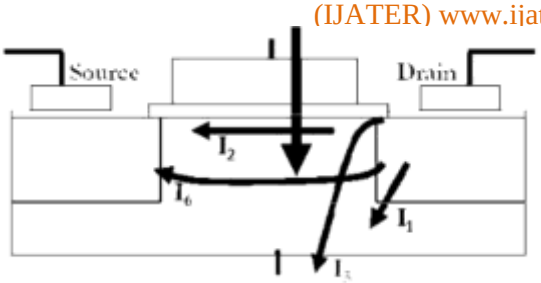
### *A. Dynamic Power Dissipation*

It can be further divided into 3 major categories as: switched power dissipation, short circuit dissipation, and glitch power dissipation all these depends much on load capacitance, supply voltage and signal timing.

### *B. Static Power Dissipation*

Static power components becomes important when the circuits are at rest then in the circuits they are all biased to the specific state of the circuit.

*1) Leakage Power:* Leakage power as a fraction of total power increases when the clock frequency falls. Scaling down of FET's requires lowering threshold voltage, which in turn increases leakage power.




**Fig(6): Leakage Power Component**

*2) Junction Leakage:* The PN junctions between diffusion, substrate and well are all junction diodes. These are reverse biased as substrate is connected to ground and well is connected to Vdd. But reverse bias leads to small amount of current.

**Fig (7): Junction leakage due to reverse biasing.**

# POWER REDUCTION TECHNIQUES FOR VARIOUS POWER DISSIPATING COMPONENTS

In the beginning of last decade, battery powered hand held devices evolved rapidly. This called for low power operation and lot of design methods on different hierarchy levels.

### *A. Voltage Scaling And Reduced Voltage Swing*

Reducing the supply voltage is an attractive solution to reduce the power dissipation since both the switched and the short circuit power dissipation have a strong dependence on threshold voltage (Vth). Another way of sustaining the throughput is to do an architectural voltage scaling.

### *B. Clock Frequency Reduction*

Reducing the clock frequency is not as beneficial as reducing supply voltage. However many processors in now a days have different power down modes where the clock signal is inactive to block the application that are unused at that moment. This process is known clock gating which can be used in most cases as conjunction with other low power techniques.

### *C. Switched Capacitance Reduction*

Reducing the switched capacitance is similar power efficient as reducing the clock frequency of the circuit. Many advanced techniques have been proposed to reduce the switched capacitance. The selection of logic style can significantly affect the critical capacitances.

The table below shows energy comparison by varying Vdd and frequency:

| Voltage ($V_{dd}$) | Frequency (f) | Power ($P_d$) | Energy ($E_d$) |
|---|---|---|---|
| $V_{dd}$ | $f_{max}$ | $P_d$ | $E_d$ |
| $V_{dd}/2$ | $f_{max}$ | $P_d/4$ | $E_d/4$ |
| $V_{dd}/2$ | $f_{max}/2$ | $P_d/8$ | $E_d/4$ |
| $V_{dd}$ | $f_{max}/2$ | $P_d/2$ | $E_d$ |

**Table1:**

*D. Method To Modulate IS Leakages*

We can reduce reverse IS leakage by varying the bias voltage both for high and low threshold voltage devices as given below

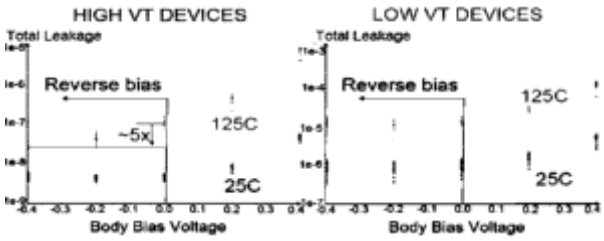



**Fig (8): High and low Vth devices with respect to leakage current.**

*E. Reducing Gate Leakage Using Nitrogen And High K*

Gate current depends more on dielectric material concentration (K) and temperature. We can limit gate current leakage by scaling appropriate material by selective use of ultra-thin surface modification layers and increased nitrogen concentration. Optimized dielectric stack reduces threshold shift by 200 to 300mV.Leakage current variation is in the diagram and graph is the variation of gate voltage wrt capacitance density.

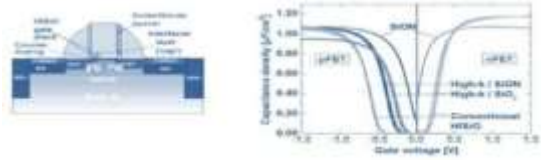


**Fig (9): gate vtg v/s capacitance density**

*F. Methods To Reduce Junction Leakages*

Leakage modulation is primarily done at transistor doping level and band to band tunneling increases with doping levels.

# VLSI CIRCUIT DESIGN TECHNIQUES FOR LOW POWER

*A. Adiabatic Circuits*

In adiabatic circuits power is reused instead of dissipating. It can be done by externally controlling length and shape of signal transitions. Diodes are not used in the design of adiabatic circuits because of thermodynamically irreversible in nature. MOSFET's are not switched on when there is a potential difference between source and drain voltages and should not be turned off when there is a small amount of current flow in the circuit.

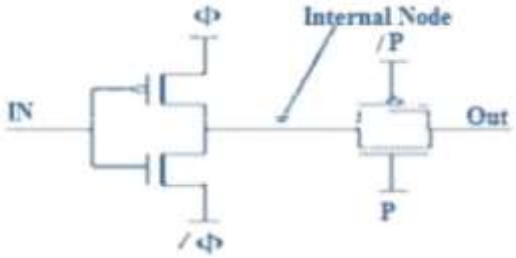



**Fig (10): Adiabatic circuit- charge recovery logic**

From the fig (10) /P and ¢ are at Vdd similarly P and / ¢ are at Vss. Pass gate P is turned off as soon as output is sampled.

*B. Logic Design For Low Power*

In case of static CMOS circuits power dissipation due to short circuit current is about 10% of total power consumption. But in dynamic CMOS we eliminated this problem since there is no direct DC path from supply voltage to ground.

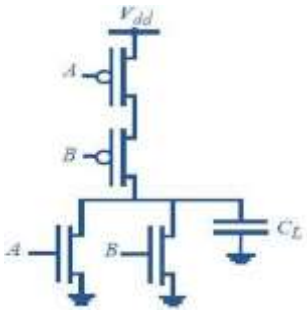



**Fig (11.a) Static Circuit (NOR gate)**

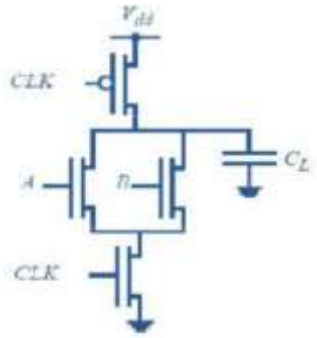



**Fig (11.b) Dynamic Circuit (NOR gate)**

*C. Reducing Glitches*

Glitches usually occurs when two parallel driving common gate arrive at different times. This leads to incorrect output before resulting the actual one. The glitches can be reduced by using buffer circuit as shown below.


**Fig (12): Buffer circuits**

*D. Logic Level Power Optimization*

Power optimization is done by adjusting the parameters such as supply voltage and size of the gates path equalization by using buffer insertion, remapping transformation where high active node is removed and replaced by new mapping onto an AND or OR gate.

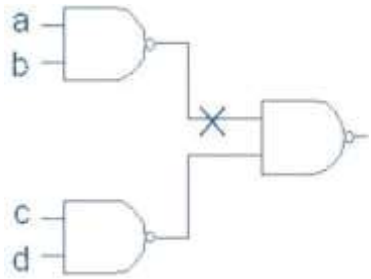



**Fig (13): Remapping transformation**
**In the fig 'X' indicates high active node**

*E. Standby Mode Leakage Supression*

Leakage power originates from substrate currents and sub treshold leakages. Multiple treshold and variable treshold circuit techniques are often used to meet leakage power constraints.

*F. Variable Body Biasing*

Variable threshold dynamically control threshold voltage of transistors through substrate biasing and hence overcome shortcoming associated with multi threshold design circuits. This can be used only when variable threshold circuit is in standby mode and in the circuits NMOS is negatively biased where as PMOS positively biased to reach Vth.

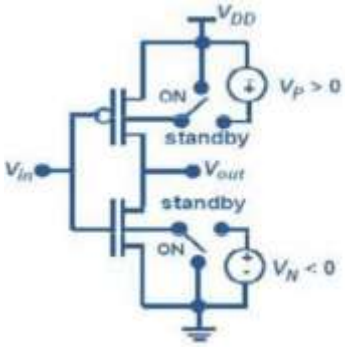



**Fig (14): Variable body biasing.**

When circuit is in standby mode both the MOS's are biased by third supply voltage to increase Vth as shown in the fig (14).

*G. Sleep Transistors*

Sleep transistors are high threshold voltage transistors connected in series with low Vth devices. When low Vth devices are ON sleep transistors will also be ON resulting normal operation. Since high Vth in series with low Vth leakage power is measured across high Vth devices thus resulting in lowering the static power dissipation.

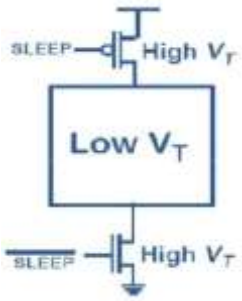



**Fig (15): Sleep transistors**

*H. Short Circuit Power Suppression*

When pairs of PMOS and NMOS transistors are conducting simultaneously it leads to short circuit current then into short circuit power. The methods to reduce short circuit losses is to keep the input and output rise or fall time same. If Vdd<Vtn+|Vtp| then short circuit power can be eliminated. Similarly when load capacitance is very large output fall

time is larger in comparison with input rise time then drain-source voltage of PMOS will be zero thus short circuit power also zero.

# CONCLUSION

Power consumption is associated with load capacitance, operation frequency, clock speed, supply voltage, threshold voltage, gate current and other factors like input and output rise time, output loading affect. Reduction of any of these is beneficial and provides economic, reliable circuits extended battery life of the electronic devices and helps to overcome problem associated with high temperature and need of heat sinks.

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