DESIGN OF LOW POWER PHASE LOCKED LOOP IN SUBMICRON TECHNOLOGY

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Abstract

This paper presents design of phase locked loop system for low power applications. The design focuses on reducing power consumption. This design consists of low power phase frequency detector, low jitter charge pump, fully differential Ring oscillator based VCO along with voltage to current convertor and current controlled oscillator, 2nd order passive loop filter and 7 bit digital frequency divider using 350nm, 180nm and 130nm technology nodes at 350MHz. Results are carried out on SPICE at various technology nodes. For 3V power supply, power consumption of PLL system is reduced to 65% at 350nm technology node.

Keywords: Phase locked loop, Phase frequency detector, and charge pump, loop filter, voltage controlled oscillator, frequency divider.

Introduction

PLL is the most constituent of modern electronics system. Any timing jitter or phase noise will degrade the performance of system. Due to switching activities in digital system supply or substrate noise is introduces in the system. Low power consumption is always desired for designing any system.PLL is the most constituent of modern electronics system. A PLL is negative feedback system that locks reference signal with feedback signal [1]. Various applications of PLL include clock-and-data recovery, microprocessor clock generation and frequency synthesizer [2]. However design and implementation of PLL is more challenging as jitter is inversely proportional to power consumption, so some tradeoff between them is necessary [3].

PLL Definition

A PLL is feedback system that fixes relation between output clock phase and input clock phase. Actually phase of both input signal and output signal are synchronized or locked, hence name called **"Phase Locked Loop"** [2] as shown in Figure 1.

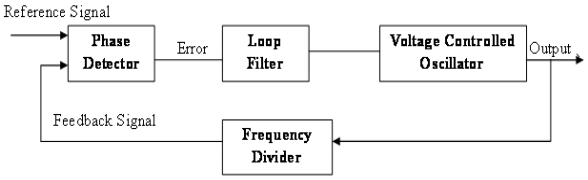


Figure 1: PLL Block Diagram

Figure 1 consists of four blocks i.e. phase detector, loop filter, voltage controlled oscillator and frequency divider. This is called 1st order PLL or Type 1 PLL. It suffers from limited acquisition range. So to eliminate this problem, Phase frequency detector along with charge pump is replaced by phase detector. Functionality of all these blocks is explained below.

A. Phase Frequency Detector (PFD)

The purpose of phase frequency detector is to detect the phase and frequency between input signal and feedback signal and generates error which is equal to phase deviation between them.

B. Charge Pump

Charge pump is a kind of DC convertor that uses capacitor as energy storage element. Signals coming from PFD are applied to charge pump to steer the current into and out of capacitor causing voltage to increase or decrease accordingly.

C. Loop filter

Output voltage from passive filter is control voltage of VCO which increase/decrease frequency in such a manner that voltage output is maintained proportional to charge of the capacitor [1].

D. Voltage Controlled Oscillator (VCO)

This is the most important block of PLL system that helps to produce output frequency according to voltage. VCO is fully differential based ring oscillator consisting of three parts i.e. voltage to current convertor, current controlled oscillator (CCO) and level shifter.

E. Loop Divider

This block provides greater flexibility to design engineers by operating PLL system at higher frequencies. Also it is used to reduce frequency coming from VCO.

Proposed PLL architecture and sub blocks

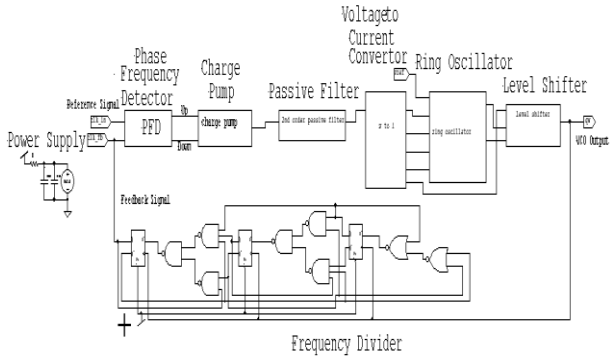


Figure 2: Proposed PLL Architecture

Proposed PLL as shown in Figure 2 consists of low power phase frequency detector when compared with existing work i.e. dynamic logic phase frequency detector [5] which consumes power of about .48mW. In this paper our proposed PLL the PFD consumes less power which is about .15mW. In addition to PFD proposed PLL consists of low jitter charge pump, passive filter, voltage to current convertor, ring oscillator (CCO), level shifter and frequency divider. All these blocks and its simulation results are explained below.

A. Implementation/Redesign of High Speed Low Power Phase Frequency Detector

The very first block of PLL system is Phase frequency detector. In this paper low power and high speed PFD is presented as shown in Fig 2.1(a) instead of traditional PFD which consists of two D Flip-flops and invertors and AND gate at feedback path. This architecture consists of two NAND Gates while eliminating reset signal and the resultant output shows corresponding up and down signals high. This circuit is implemented at 350nm, 180nm and 130nm technology nodes operating at 50MHz with power supply of 3V, 1.8V and 1.3V respectively [4].

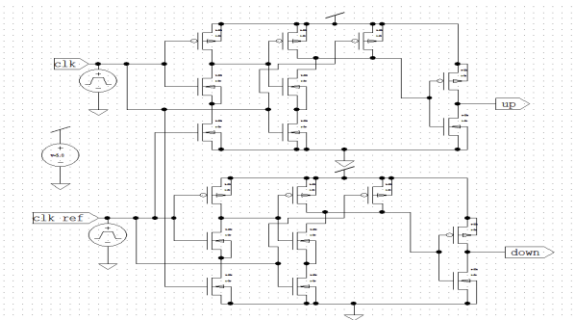


Figure 3.1(a): Redesign Phase frequency detector

Simulation results of the redesigned PFD are shown in Figure 3.1(b) which consists of up and down signals as outputs and inputs as reference and feedback signal. If the reference signal is leading feedback signal then up signal is high and varying from 0 to 3V and down signal is constant in mV. These outputs are connected to charge pump to generate corresponding output.

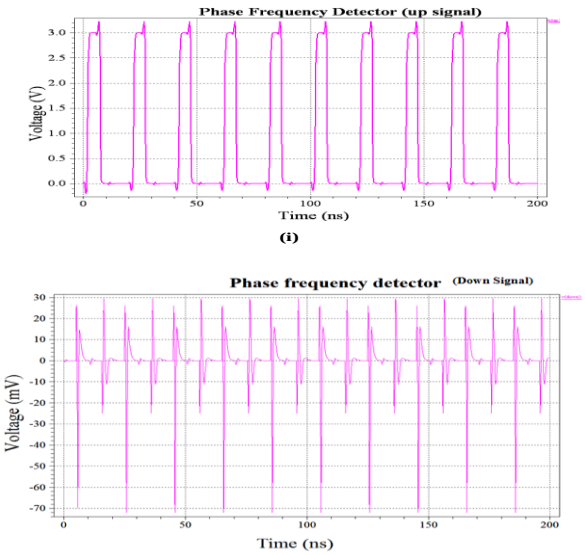
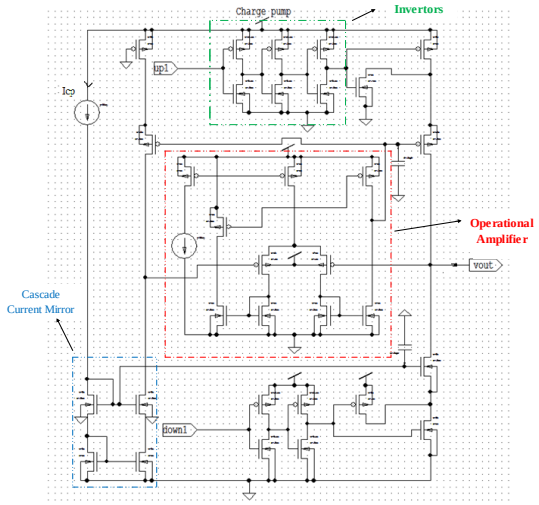


Figure 3.1(b): Output Waveform of Phase frequency detector

B. Charge pump circuit

Charge Pump is next block after phase frequency detector. The outputs *up* and *down* signals of PFD are connected directly to charge pump. Basic charge pump converts logic states of PFD output into analog signal making it suitable to control VCO frequency. A novel low jitter charge pump is designed in such a way that it removes all non idealities. When PFD output is high, current (Icp) will flow out of charge pump and charges loop filter [5]. Single ended low jitter and low power charge pump is shown in Figure 3.2.



(ii)

Figure 3.2: Charge pump circuit

C. Loop Filter

It is 2nd order passive filter consisting resistor and capacitor in series and other capacitor is used to reduce spikes which is parallel to both of them its function is to convert the current coming from charge pump to control voltage that is connected to VCO as shown in the Figure 3.3(a). Following parameters (capacitance and resistance value) are calculated from the mathematical equation.

$$Z_{loopfilter}(s) = \frac{sT_0+1}{s\,(sT_1+1)\,(C_0+C_1)} \quad (1)$$

$$T_1 = \frac{\sec(\varphi)-\tan(\varphi)}{\omega_{BW}} \quad (2)$$

$$T_0 = \frac{1}{\omega_{BW}^2 T_1} \quad (3)$$

$$C_1 = \frac{T_1 I_{Cp} K_{vco}}{T_0 2\pi T_1 N_{fd}} \sqrt{\frac{(1+(\omega_{BW})T0)^2}{(1+(\omega_{BW})T1)^2}} = 3.7pF \quad (4)$$

$$C_0 = C_1\left(\frac{T_0}{T_1} - 1\right) = 24pF \quad (5)$$

$$R_0 = \frac{T_0}{C_0} = 18K \quad (6)$$

Where Icp: Current of charge pump.
K_{vco}: Gain of VCO.
ω_{BW}= Loop bandwidth = 1.25MHz
N_{fd}=Multiplication factor.

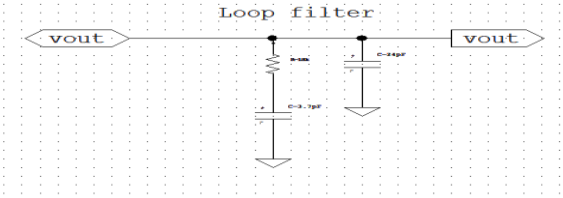


Figure 3.3 (a): Passive loop filter

Figure 3.3(a) shows charge pump output which charges and discharges according to output from PFD. Figure 3.3(b) shows phase frequency detector output when one of signal of PFD is high and in Figure 3.3(c) shows combined output of phase frequency detector and charge pump.

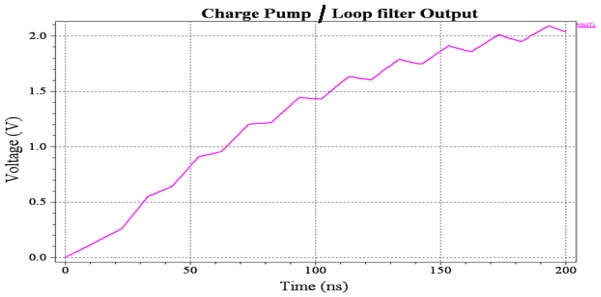


Figure 3.3(b): Charge pump/loop filter output

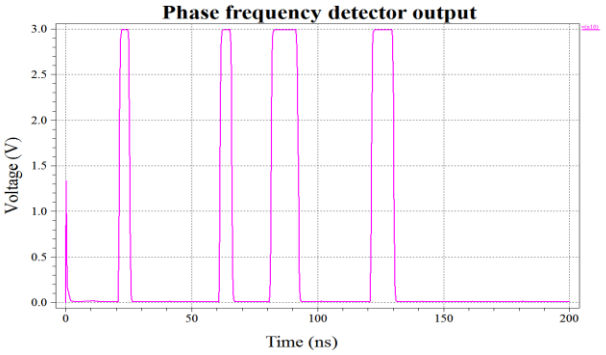


Figure 3.3(c): Phase frequency detector output

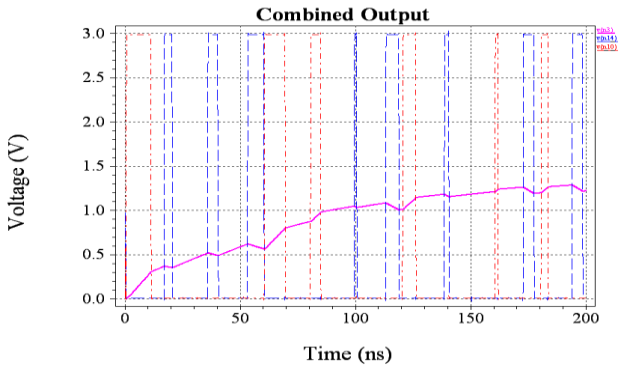


Figure 3.3(d): Combined output

D. Differential based ring oscillator

Implementation of VCO comprised of three stages. First stage is voltage to current convertor which is used to increase the current at input of current controlled oscillator in the second stage which is fully differential three stage ring

oscillator and used to decrease power consumption and last stage is level shifter used to shift the output rail to rail of CCO.

i) Voltage to current convertor

The output current of voltage to current convertor is given by:

$$I_B = \frac{V_{in}}{R0} \quad (7)$$

It consists of operational amplifier and provides biasing to current controlled oscillator along with biasing to level shifter [5-6]. Voltage to current convertor schematic is shown in Figure 3.4 (a).

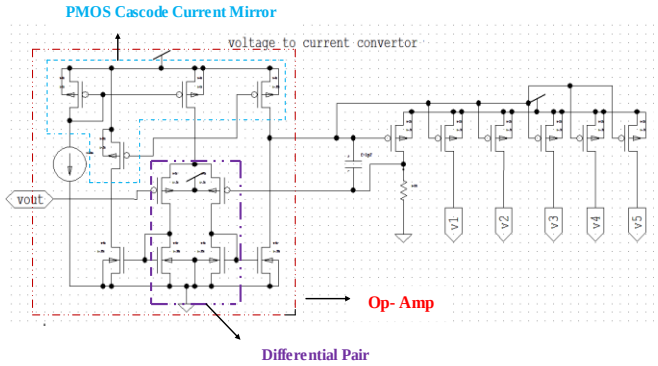


Figure 3.4(a): Voltage to current convertor

ii) Current controlled oscillator

Each stage consists of source coupled differential NMOS pair, loaded with PMOS transistor operating in triode region. Further CCO consists of replica biasing circuits for keeping output amplitude constant [5]. The schematic of CCO is shown in Figure 3.4 (b)

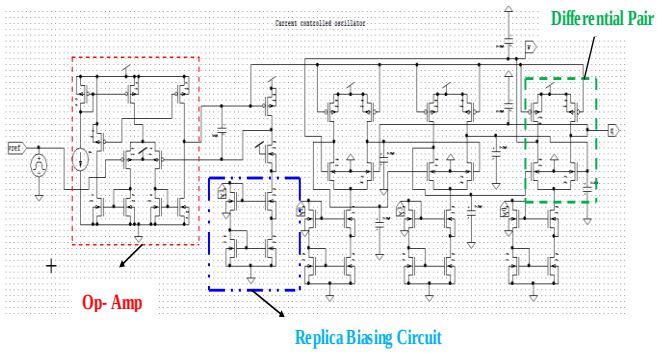


Figure 3.4(b): Current controlled oscillator

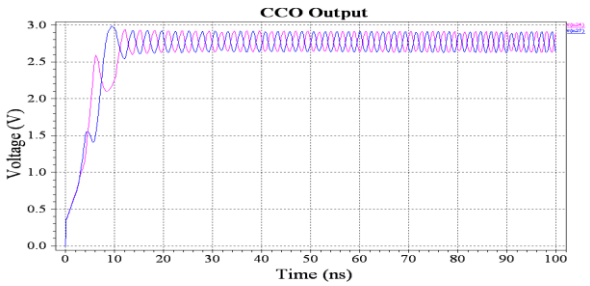


Figure 3.4(c): Simulation of Current controlled oscillator

Simulated result is shown in Fig 3.4 (c) which consists of two outputs i.e. w and q. The control voltage which is output of the loop filter and input to the VCO is ranging from 0.0V to 2V, which is applied to voltage to current convertor. The converted current from the voltage using voltage to current converter is going to CCO. Simulated results of CCO are a continuous waveform having voltage range from 2.5V to 2.9V.Simulated result of CCO is a continuous waveform having voltage range from 2.5V to 2.9V.

The nominal delay of output buffer is given as:

$$Td = \frac{V_{sw} \cdot C_L}{Ibias} \quad (8)$$

Where

V_{sw}: output swing of delay buffer
C_L: Load capacitance of delay buffer
I_{bias}: Biasing current of delay buffer

Value of output swing Vsw is calculated from graph i.e. 0.3V which is less than NMOS threshold Value.
Load capacitance C_L = 0.34pF and $Ibias$ = 20uA.

Frequency of VCO can be calculated from following mathematical expression.

$$F_{vco} = \frac{1}{2*N*Td} \quad (9)$$

N: No of stages in CCO

iii) Level Shifter

The level shifter is implemented with help of folded cascode amplifier along with differential input stage and CMOS inverter as output buffer [6]. They have the capability of pulling up and down the voltages to rails. as is shown in Figure 3.5(a) and simulated output is shown in Figure 3.5(b).

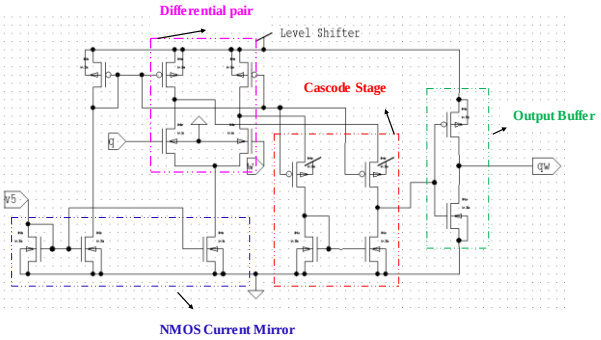


Figure 3.5(a): Level Shifter

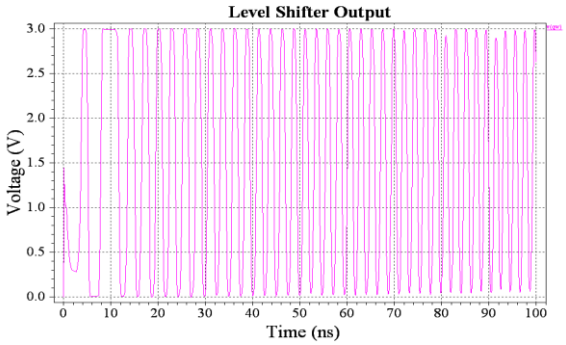


Figure 3.5(b): Simulation result of Level Shifter

E. Frequency divider

The design of frequency divider is a pure digital circuit having D Flip-Flops, NAND gate and NOR gate which is implemented from the standard cell library [6]. The schematic of frequency divider is shown in Figure 3.6(a).

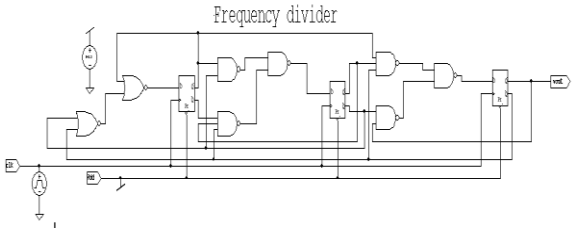


Figure 3.6(a): Schematic of frequency divider

Simulated result is shown in Figure 3.6(b) describes the output of frequency divider divides level shifter output by 7 (multiplication factor).

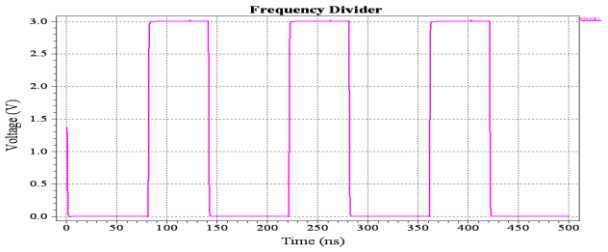


Figure 3.6(b): Simulation of Frequency detector

Power Reduction

Power is very important issue while designing PLL. Power can be reduced by using low power techniques, by scaling down voltage etc. One way to reduce power is to use decoupling capacitor. It will also reduce jitter along with power.

The following schematic is having decoupling capacitors attached with power supply [7-8] and simulation is shown in figure 3.7.

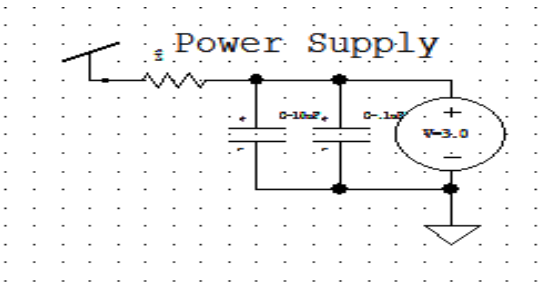


Figure 3.7: Power Supply Circuit

Experiment results

The Design is simulated at 350nm using all these parameters and following are the design specification is shown in TABLE 1.

Table 1. Design specification of PLL

Parameters	Value
Reference Frequency	20MHz-2GHz
Current of Charge pump (I_{cp})	20μA
Gain VCO (K_{vco})	220MHz/V
Loop bandwidth(ω_{BW})	1.25MHz
Output Frequency	350MHz-14GHz
Multiplication Factor	7
R,C_0,C_1	18k,24pF,3pF

Table 2. Comparison of various parameters at different technology nodes

Parameters	350 nm [5]	350 nm	**350 nm (optimized results)**	180 nm	130 nm
Supply Voltage(V)	3.3	3.0	**3.0**	1.8	1.3
Power (mW)	12	9.6	**7.6**	2.2	1.4
Max power (mW)	63	45	**31**	18	9
Min Power (mW)	16	12	**12**	3.7	4
RMS Value (V)	2.3	1.9	**1.7**	1.1	0.8
Average Value (V)	1.8	1.5	**1.3**	0.9	0.5
VOL (mV)	-8.3	-3	**-0.8**	-0.1	-0.08
VOH (V)	3.3	2.99	**2.8**	1.7	1.2
IDD (mA)	3.6	3.5	**2.9**	1.7	0.9

Conclusions

This paper presents low power PLL design at 350nm technology node. With improved low phase frequency detector and decoupling capacitor, the power consumption of the proposed PLL is reduced to 65% at 350MHz nominal frequency for 3V power supply. With 180nm and 130nm technology nodes power consumption is reduced to 2.2mW and 1.4mW at 1.8V and 1.3V respectively.

Acknowledgment

As with any enterprise, this research work could not have been completed without help and support of others. I would like to thanks my research advisor Mrs V.Sulochna Verma for their valuable contribution. Finally I wish to thank my family and friends for their support and encouragement.

References

[1] Abishek Mann "The Design of a Low-Power Low-Noise Phase Lock Loop", IEEE Proceedings of ISQED.2010.5450522, April 2010.

[2] Feng Lin "Research and Design of Low Jitter, Wide Locking-Range All-Digital Phase-Locked and Delay-Locked Loops" PhD Thesis, Electrical Engineering, March 2000.

[3] Mohegan Mansuri "Low-Power Low-Jitter On-Chip Clock Generation" PhD Thesis, Electrical Engineering, UCLA, 2003.

[4] Kruti P. Thakore "Low Power and Low Jitter Phase Frequency Detector for Phase Lock Loop" International Journal of Engineering Science and Technology (IJEST), Volume: 3, 2011.

[5] Kilian Imfeld "Low-Jitter and Low-Power CMOS PLL for Clock Multiplication", Solid-State Circuits Conference, 2006. ESSCIRC 2006, pp-174-177.

[6] Xintian Shi "Design of Low Phase Noise Low Power CMOS Phase Locked Loops" PhD Thesis, Soutenue LE 20 NOV 2008.

[7] Mariajose Perez Ferrando "Power Supply Rejection to Noise in Sinusoidal Clock Buffers: CDC3S04, Texas instrumentation, June 2010.

[8] Kal Mustafa "Filtering Techniques: Isolating Analog and Digital Power Supplies in TI's PLL-Based CDC Devices, Texas instrumentation, October 2001.

[9] Yutao Liu"Power and Jitter Optimized VCO Design Using an On-Chip Supply Noise Monitoring Circuit," IEEE Proceedings of 978-1-4244-7456-1, pp-939-940, 2010.

[10] Julien Roche "A Low-Noise Fast-Settling Phase Locked Loop with Loop Bandwidth Enhancement," IEEE Proceedings of 978-1-4244-2332-3, pp-165-168, 2008.

[11] Adnan Gundel "High Performance Low Phase Noise PLL Clock Synthesizer with LVDS Outputs" IEEE paper. Systems, Applications and Technology Conference, 2006.LISAT 2006.

[12] Todd Wey "A Circuit Technique to Improve Phase-Locked Loop Charge Pump Current Matching" IEEE-NEWCAS Conference,pp- 235 – 238,june 2005.

Bibliographies

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