CMOS ULTRASOUND TRANSMITTER CHIP USING VERILOG-A

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Abstract

The proposed CMOS ultrasound transmitter chip will enable the development of portable high resolution, high-frequency ultrasonic imaging systems. A prototype design containing 16 transmit channels is with DPLL and Delay block. The ultrasound imaging system used in medical application is very huge and bulky which is impossible for portability, CMOS ultrasound transmitter which enables the ultrasound imaging system to be a portable system. Only transmitter does not help in portability a transmitter with receiver will make a system portable. Here we propose the CMOS ultrasound transmitter chip which work with 5V and 40MHz. In addition, transmit digital beamforming system architecture is supported in this work. The design and measured simulation results are given in this work. The design and measured simulation results are given.

Keywords: Ultrasound Transmitter, DPLL, PDF,

I. Introduction

Ultrasound imaging has overtaken X-ray imaging as the most widely used medical imaging technique because it is noninvasive, exhibits very good lateral and axial resolution, and is less expensive than other imaging modalities. 50MHz. For example, frequencies between 1and 10MHz are used in diagnostic imaging applications which penetrate tissues depths of 5–20cm. For higher frequency ranges between 20–50MHz, ultrasound is used for imaging smaller organs or surfaces such as skin, the gastrointestinal tract, and intravascular imaging of blood vessels. Although the majority of medical ultrasound imaging is performed between 1 and 50MHz, there is a need for better clinical ultrasound imaging for detecting early skin cancer and many other diseases in vivo without the use of biopsy. Imaging techniques with a Resolution below 100µm is required for this purpose.

In addition, there is a recent demand for portable ultrasound imaging systems in medical services. For example, veterinarians can use a portable ultrasound imaging for onsite diagnosis of pets and Emergency Medical Technicians (EMT) can utilize this technology at accident scenes. The conventional ultrasound imaging system, however, is still reasonably large and not suitable for mobile devices because it uses high voltage (up to 100 V) transducers and complicated front-end electronics consisting of discrete IC chip sets of pulsars, preamplifiers, time gain control (TGC), analog-to-digital (A/D) converters, and memory devices.

A novel, portable, high-resolution ultrasound imaging system with MEMS transducer arrays...
has been proposed. The ultrasound imaging system has a micron-scaled high-frequency (30~150MHz) transducer array which operates with 3~5V power supplies and a full custom designed CMOS transmitter chip. The system utilizes highly integrated electronics close coupled with thin film piezoelectric elements on larger MEMS structures as the transducers. It is anticipated that this will enable the ultrasound imaging system to be portable and compact while maintaining high image resolution.

Verilog-A, which is studied in this paper, is one of the most excellent top-down hardware description language specifically for analog and mixed signal designs.

Our paper consists a transmitter chip and its specification. Section II comprises of DPLL (Digital Phase Lock Loop) block diagram. Section III consists of block diagram of the transmitter. The implementation of transmitter is present in section IV. We have concluded our work in the last section V.

II. Digital Phase Lock Loop

DPLL is a circuit that is used frequently in modern integrated circuit design. A DPLL circuit may consists of a serial shift register which receives digital input samples (extracted from the received signal), a stable local clock signals which supplies clock pulses to the shift register to drive it and a phase corrector circuit which takes the local clock and regenerates a stable clock in phase with the receiver signal by slowly adjusting the phase of the regenerated clock to match the received signals.

In this transmitter timing is a crucial part and the perfectness of the input pulse to the transmitter is very important so to achieve the perfect pulse we use DPLL frequency synthesizer. The figure 1.1 shows the block diagram of the DPLL.

This DPLL circuit is conventionally based on three essential components,
1. Phase Frequency Detector (PFD)
2. Loop Filter (LF)
3. Voltage-Controlled-Oscillator (VCO)

II.I PHASE FREQUENCY DETECTOR

The phase detector first compares the differences between the input signal and the VCO output signal. It then generates a phase error according to the difference. It then generates a phase error according to the difference. Passing through the loop filter, the feedback loop will present a control signal for the voltage-controlled oscillator to either increase or decrease the oscillating frequency. In accordance to the controlled voltage level. Recursively, the entire
phase-locked loop will be able to lock the input signal within a lock-in time. It compares the leading edges of the input data (from the feedback circuit) and the reference clock and the width of the two inputs does not matter here. For understanding purpose let us consider a example shown in figure 2.2. In figure 2.2(a) the data leads the clock rising edge the “Up” output of the PFD goes high. In figure 2.2(b) the data lags the clock rising edge the “Down” output goes high. In figure 2.2(c) the rising edge of both the inputs of the PFD are rising at a same time so Up and Down both remain low.

As there are two outputs from the PFD we need to combine into a single output for further block as they contain single input. Here we use a tri-state output to combine the outputs of the PFD. When both the signals Up and Down are low, both the MOS-FETs are off and the output is in high-impedance state. If the Up signal goes high the pmos turns on and pulls the output up to VDD, while the Down signal is high, the output is pulled low through nmos.

**II.II LOOP FILTER**

The loop filter is the brain of the DPLL. The values for the loop filter is to be selected carefully and correctly, if not it may take the loop too long to lock, or once locked, small variations in the input data may cause the loop to unlock. This loop filter is nothing but a low pass filter which passes only low frequency and avoids high frequency.

**II.III VOLTAGE CONTROL OSCILLATOR**

A voltage-controlled oscillator (VCO) is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. The frequency of oscillation is varied by the applied DC voltage, VCO has the feature that it’s oscillating frequency on the output port is under controlled by the input control voltage.

![Figure 2.3: PFD inputs and outputs](image)

**III. Transmitter**

Modern ultrasound imaging systems are often based on the digital beamforming (DBF) system. It uses multi-channel transducer arrays to increase beam energy, and to enhance the resolution. The CMOS transmitter chip, based on a typical DBF system, has 16 transmit channels, each transmit channel has variable pulse length and a delay element for transmit beam focusing. The transmit signal generator produces and sends a 160-MHz pulse to the MEMS transducers through programmable delay chains to enable electronic beam focusing in the transmit mode. In a DBF system, focusing is achieved by introducing delays to the transmit pulse.
on the elements so that emitted ultrasonic beams can be made to interface constructively at the target of interest. Therefore, excitation pulses should be delivered to the transducer elements in such an order that a composite wave front converges to a point.

the output as 010101… So this type of output is given by this D flip-flop. The block diagram is shown in the figure 3.1 of single delay and D flip-flop block

Our transmitter system consists of a delay block and a D flip-flop. The delay needed for the generated pulse to focus on the focal point at same time. As we need 16 channels we use D flip-flop to give us p-channel and n-channel. If p-channel gives the output as 101010….. the n-channel should give

IV. Implementation and Results

As we said before the implementation of each and every block is done in Verilog-A language it is done in cadence software using virtuoso tool. The implementation and results are shown in below.
Figure 4.3: Circuit Design of Transmitter

Figure 4.4: Waveform of Transmitter Channel 1 to 4 with input

Figure 4.5: Waveform of Transmitter Channel 5 to 10

Figure 4.6: Waveform of Transmitter Channel 11 to 16
V. Conclusion

An integrated CMOS transmitter chip has been designed for high-resolution ultrasonic imaging system. A 16-channel analog front-end consisting of a transmit Beamformer is implemented in cadence software. For a transmitting the signal the time is a crucial part the signal focusing at the focal point must be at same time so for delay to the channels is given by delay program and to create a 16 channel a D flip-flop is used. To give a input to the transmitter a DPLL is used which gives a perfect pulse without a phase error.

VI. References


Biographies

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